A Method Of Forming A Structure Wherein An Electrode Comprising A Refractory Metal Is Deposited

Cross Reference to a Related Application

This application claims the benefit of US Provisional Patent Application 60/454,905 filed March 14, 2003, the disclosure of which is hereby incorporated herein by reference.

Technical Field

The presently disclosed technology relates to a method for forming a structure wherein a gate comprising a refractory metal is deposited. More specifically, the presently disclosed technology relates to a method for forming a structure wherein a gate comprising a refractory metal, and having a mushroom shape is deposited.

Background

Previously, attempts have been made at forming mushroom shaped gates of field effect transistors using refractory metals. Mushroom shaped gates typically have a large cross-sectional area to reduce resistance, while the portion of the gate contacting the substrate remains small to reduce capacitance. As a result, transistors with mushroom shaped gates have desirable high-frequency and low-noise characteristics. Typically, mushroom shaped gates are fabricated by forming a mold in several electron sensitive resist layers, wherein metal for the gate could be deposited. However, these resist layers would generally deform if a refractory metal was deposited because of the high temperatures needed to deposit refractory metals, rendering the attempt unsuccessful. As a result, metals such as aluminum and copper are commonly used in the industry because they can be evaporated at a temperature sufficiently low, so that the resist is unaffected. One disadvantage of not using a refractory metal is that high temperature processing cannot be performed after forming the gate. Typical non-refractory gate metals include

gold, aluminum, and copper. After the gate has been formed using one of these metals, the metal may diffuse into the substrate if exposed to high temperature processes. These high temperatures are not necessarily the melting point of the metal, but merely high enough to allow the metal to diffuse into the substrate. In addition, gates with these metals have a tendency to diffuse into the substrate over extended periods of time, even without the presence of high temperatures. However, by depositing a refractory metal between the gate and the substrate, the diffusion problem can be avoided.

Prior attempts at incorporating a refractory metal have been attempted, but resulted in complicated techniques. U.S. Patent 5,739,557 O'Niel, LL, et al., "Refractory Gate Heterostructure Field Effect Transistor," teaches the fabrication of a HFET using a refractory metal gate and a refractory ohmic contact. However, the fabrication scheme disclosed does not allow a metal lift-off step to remove the resist after the gate is formed. This significantly complicates the process. This fabrication scheme requires the use of dielectric deposition and etching techniques which add complexity to device processing and limit its use to materials which are compatible with these techniques. A similar non-lift-off refractory gate fabrication scheme is discussed in T. Suemitsu et al. in Jpn. J. Appl. Phys. Vol. 37 (1998) Pt. 1 No. 3B pp. 1365-1372. Suemitsu describes the fabrication of a refractory metal sub 0.25 micron gate using multiple dielectric layers with multiple reactive ion etching steps and sputtered metal films in a non-lift-off process. As with O'Niel, LL, et al., this technique requires the use of dielectric deposition and etching techniques which add complexity to the process.

As a result, there is a need for a simple process in which a structure is fabricated, wherein a gate comprising a refractory metal can be deposited, followed by removal of resists and extraneous metals using a simple lift-off process.

Summary

The presently disclosed technology addresses the aforementioned needs by providing a method for forming a structure wherein a gate comprising a refractory metal

is deposited. The applicant has experimentally determined that a commercially available resist marketed as having a high resistance to reactive ion etching may also have the necessary properties needed to prevent resist deformation during exposure to the high temperatures needed for refractory metal deposition.

Accordingly, in one aspect of the presently disclosed technology, a substrate is provided and a plurality of electron sensitive resist layers are deposited over the substrate. Two layers in the plurality of resist layers will not deform when exposed to the high temperatures needed for refractory metal deposition. Using electron beam lithography, specified regions in the resist layers are defined. The defined regions are then developed to remove the defined regions from the resist layers, thereby creating a mold in which a gate can be deposited. If desired, a recess can be etched into the substrate. A refractory metal is then deposited in the mold on the substrate followed by a gate contact to form the gate. After the gate is formed, a lift-off process is used to remove the plurality of resist layers.

In another aspect of the presently disclosed technology, a plurality of alignment markers are preferably deposited on the substrate surface to help more accurately define an area in resist layers in which a mold is formed. Because of the thickness and characteristics of the plurality of resist layers, it is necessary to expose and remove through development an area above and around the alignment markers to provide for accurate pattern registration. The alignment markers preferably comprise ohmic metal and are exposed by removing the portion of the resist layers directly above and around the alignment markers. The electron beam machine then uses the alignment markers as a reference point for exposing the regions of the resist layers where the mold is to be formed.

Brief Description of the Drawings

Figs. 1a-1d show a cross section of the deposited resist layers on the substrate;
Figs. 1a-1 and 1a-2 show a top view of the substrate with the alignment markers;

Fig. 1e shows the defined regions above the alignment markers;

Fig. 1f shows the defined regions above and around the alignment markers removed;

Fig. 2a shows a cross section of the defined regions in the second and third resist layers;

Fig. 2b shows a cross section of the defined regions in Fig. 2a removed from the second and third resist layers;

Fig. 2c shows a cross section of the defined region in the first resist layer;

Fig. 2d shows a cross section of the defined region in Fig. 2c removed from the first resist layer;

Fig. 2d-1 shows a recessed region formed in the substrate;

Fig. 3a shows a cross section of molybdenum deposited in the gate contact region and gate foot region;

Fig. 3a-1 shows a cross section of an enlarged version of Fig. 3a;

Fig. 3b a cross section of gold deposited on the molybdenum; and

Fig. 3c shows a cross section of the gate after lift-off.

Detailed Description of the Disclosed Technology

The presently disclosed technology will now be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the technology are shown. This presently disclosed technology may be embodied in many different forms and should not be construed as limited to the embodiments set forth herein.

The presently disclosed technology provides a method for forming a structure wherein a metal electrode (such as a gate of a field effect transistor) comprising a refractory metal is deposited. Accordingly, a substrate is provided, whereon first, second, and third resist layers are sequentially deposited. The first and third resist layers are able to maintain their shape when exposed to the high temperatures needed to deposit the refractory metal. The second resist layer may show some deformation when exposed to high temperatures, however, because it is sandwiched between the first and third resist

layers, it will generally be able to maintain its shape when exposed to high temperatures. The second resist layer should, however, be of a viscosity so as to allow it to form a layer thicker than either the first or third resist layers to be applied. Electron beam lithography is then used to define regions in the resist layers, which define a mold. The defined gate regions are removed from the resist layers using developer to create the mold. If desired, a recess can be etched into the substrate. Then, using metal evaporation, a refractory metal is deposited in the mold followed by a gate contact.

A preferred embodiment is now described with reference to Figs. 1-3c. In this preferred embodiment a substrate 2 is provided, as shown in Figure 1a. The substrate 2 may comprise a series of epitaxially deposited layers of group III-V materials such as InP and GaN and preferably has alignment markers 3 (discussed later) outlining a square or triangular shape on the surface 2a of the substrate 2 as shown in Figs. 1a-1 and 1a-2. The substrate 2 is preferably pre-baked at 180 °C for two minutes to ensure that the surface 2a of the substrate 2 is dry. After pre-baking, a first electron sensitive resist layer 4 is spin coated over the surface 2a and the alignment markers 3 at a suitable speed, such as 5000 RPM, to obtain a desired thickness of about 2000Å, as shown in Fig. 1b. The first resist layer 4 preferably comprises the resist sold under the tradename ZEP520-12 by the Zeon Corporation of Tokyo, Japan. After deposition, the first resist layer 4 is baked at about 180 °C for about 30 minutes. This helps solidify the first resist layer 4 after deposition and ensures that it has a smooth surface. A resist such as ZEP520-12 is preferred because it can maintain its shape when exposed to temperatures up to 180 °C, which is necessary for the deposition of refractory metals such as molybdenum.

Next, a second electron sensitive resist layer 6 is spin coated over the surface of the first resist layer at a suitable speed, such as 2500 RPM, to obtain a desired thickness of about 7000Å, as shown in Fig. 1c. The second resist layer 6 preferably comprises the resist sold under the tradename MMA(17.5)-MAA EL11 by the MicroChem Corporation of Newton, Massachusetts. A resist such as the aforementioned EL11 is preferred for the second resist layer because it has a sufficiently high viscosity to allow a layer about 7000Å thick to be deposited. Such a thick layer is needed in order to create a second

region 6a (see Fig. 2a) in which a gate contact region (discussed later) can be formed. Unlike ZEP520-12 though, the second resist need not be as resilient to high temperatures. However, because the second resist layer is sandwiched between the first and third resist layers 4, 8, it will generally not deform when exposed to high temperatures. Furthermore, it is not as critical for the gate contact to retain the contours of the mold, as it is for the gate foot and gate opening (discussed later), which are defined by the first and third resist layers 4, 8. After deposition, the second resist layer 6 is baked at about 180 °C for about 30 minutes to help solidify the second resist layer 6 and ensure a smooth surface.

A third electron sensitive resist layer 8 is then spin coated over the second resist layer 6 at a suitable speed, such as 5000 RPM, to obtain a thickness of about 3000Å, as shown in Fig. 1d. The third resist layer 8 preferably comprises the resist sold under the tradename ZEP520-22 by the Zeon Corporation of Tokyo, Japan. A resist such as ZEP520-22 is preferred for the third resist layer 8 because it can maintain its shape at temperatures up to about 180° C which are needed for the deposition of a refractory metal, such as molybdenum. Furthermore, ZEP520-22, which is similar to ZEP520-12, is far more sensitive to electron exposure during electron beam lithography than ZEP520-12, the consequences of which are discussed later.

After the third layer of resist 8 has been applied, electron beam lithography is used to define regions in the resist layers 4, 6, 8 which will be removed to create a mold for the gate. In a first exposure, the portion of the resist layers 4, 6, 8 immediately above and in a 50 micron square region around the alignment markers 3 is removed. As aforementioned, the alignment markers 3 are preferably deposited on the substrate 2 in a square pattern or triangular pattern (see Figs. 1a-1 and 1a-2). The alignment markers 3 shown in Figs. 1a-1 and 1a-2 have not been drawn to scale, but are depicted for illustrative purposes only. The alignment markers 3 have two purposes: 1) they outline the area (indicated by the dashed lines) which will be further processed to define a mold; and 2) they serve as a reference point for the electron beam machine during subsequent processing steps. As the electron beam machine scans over the resist layers 4, 6, 8, it emits a signal. The alignment markers reflect the signal back to the electron beam

machine to indicate to the electron beam that it is above an alignment marker 3, thereby serving as a reference point. The alignment markers 3 comprise an ohmic metal and preferably have dimensions that are about 20 μm^2. The spacing between alignment markers 3 mapping out an area is preferably about 10mm. To remove the resist layers 4, 6, 8 directly above and around the alignment markers 3, data including the distance between the alignment markers 3, and the shape used by the alignment markers 3 to map out an area (triangular, square) are provided to the electron beam machine. The electron beam machine then scans over the substrate surface 2a and emits an electron beam with energy of about 300 $\mu C/cm^2$ when above the alignment markers 3 to define regions in the resist layers 4, 6, 8, as shown in Fig. 1e. These regions are typically about 50μ wide. The substrate 2 is then developed in a suitable resist developer, such as 100% Methyl iso-Butyl Ketone (MIBK), for about 60 seconds to remove the defined regions in the resist layers 4, 6, 8, as shown in Fig. 1f.

The resist layers 4, 6, 8 then undergo a second exposure which defines a third region 8a in the third resist layer 8 and a second region 6a in the second resist layer 6 shown in Fig. 2a. Note the cross section depicted by arrows A in Fig. 2a and the cross section depicted by arrows A in Fig. 1f. The third region 8a is used to define a gate opening region and the second region 6a is used to define a gate contact region. To define the second and third regions 6a, 8a, the second exposure is performed by impinging electrons with an energy in the range of 38-45 $\mu C/cm^2$ onto the exposed surface of the third resist layer 8. The electrons impinging on the surface of the third resist layer 8 define an area, for example, of about 0.4 microns wide, by using the alignment markers 3 as reference points. Defining an area about 0.4 microns wide is generally known to those skilled in the art, and can be performed by adjusting the electron beam spot size, electron beam stepping distance, and computer aided design defined dimension of the electron beam machine. Once such electron beam machine that could be used is the Leica EBPG4V available from Leica Microsystems. The emitted electrons travel through the resist layers 4, 6, 8 towards the surface 2a of the substrate 2 in a direction orthogonal to the surface 2a. When the emitted electrons hit the surface 2a they are reflected back through the resist layers 4, 6, 8. However, some of the reflected electrons reflect at an

angle off of their incident angle as is figuratively depicted by arrows B in Fig. 2a. Shown in Fig. 2a is the third region 8a in the third resist layer 8, and the second region 6a in the second resist layers 6. However, there is no region defined in the first resist layer 4 by the electrons. The reason for this is that ZEP520-12 is far less sensitive to electrons than EL11 or ZEP520-22, and is essentially unaffected by electrons having energy in the range of 38-45 $\mu C/cm^2$.

The second region 6a in the EL11 is significantly larger than the third region 8a in the ZEP520-12, and has a trapezoidal shape. This is due to the fact that electrons from the second exposure are reflected off the surface 2a at angles off of the incident angle, and enter the second resist layer 6. The portion of the second resist layer 6 nearest the surface 2a receives the bulk of the reflected electrons, while the portion of the second resist layer 6 nearest the third resist layer 8 receives fewer reflected electrons, and those reflected electrons have less energy. As a result, the second region 6a generally has a cross-sectional shape which is wider at the boundary of the first resist layer 4 than it is at the boundary with the third resist layer 8. Thus, the shape is somewhat trapezoidal in cross section. It is possible for the third region 8a to receive some reflected electrons. However, because the third region 8a is farthest from the surface 2a, the reflected electrons received by the third region 8a will be significantly less in quantity and in energy. As a result, the third region 8a may be slightly widened in the portion of the second region 8a nearest the surface 2a, but in practice, the portion of the third region 8a on the side away from region 6a will not be widened significantly.

The third region 8a in the third resist layer 8 is then developed in a suitable resist developer, such as solution of 100% MIBK, for a suitable period of time, such as 360 seconds. This removes the resist in the third region 8a from the third resist layer 8, as shown in Fig. 2b, thereby forming a gate opening region 8b. Next, the second region 6a in the second resist layer 6 is developed in a suitable resist developer, such as a solution of one part Ethylene glycol monoethyl ether acetate (EGMEA) : five parts Ethanol (~~ETHO~~) (ETOH), for a suitable period of time, such as 45 to 70 seconds. This removes the resist

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in the second region 6a from the second resist layer 6, thereby forming a gate contact region 6b.

Next, a third exposure is used to define a first region 4a in the first resist layer 4, as shown in Fig. 2c. The first region 4a is used to define a gate foot region (discussed below), which will be the region where the gate contacts the substrate 2. Using electron beam lithography, a beam of electrons having energy of about 800 $\mu C/cm^2$ is directed at the surface of the first resist layer 4 in an area of, for example, about .05 microns wide. Defining an area about 0.05 microns wide is known to those skilled in the art and can be performed by adjusting the electron beam spot size, electron beam stepping distance, and computer aided design defined dimension of the electron beam machine. It is worth noting that the energy used in this third exposure is greater than the energy used in the second exposure by a factor of roughly 20. ZEP520-12 used in the first resist layer 4 is significantly less sensitive to electrons than EL11 used in the second resist layer 6 or ZEP520-22 used in the third resist layer 8. The impinging electrons from the third exposure on the surface of the first resist layer 4 define a first region 4a that is about .05 microns wide.

The first region 4a in the first resist layer 4 is then developed in a suitable resist developer, such as a solution of one part MIBK: two parts iso-propyl alcohol (IPA), for a suitable period of time, such as 60-90 seconds, thereby forming a gate foot region 4b shown in Fig. 2d. When the electrons hit the surface 2a of the substrate 2, they can reflect back through the first resist layer 4 and enter the second and third resist layers 6, 8. However, the developer used to remove the third region 4a in the first resist layer 4 does not affect the second and third resist layers 6, 8. The gate foot region 4b is noticeably smaller than the gate contact region 6b, in order to define a mushroom shape. This will allow the subsequently deposited gate to assume a mushroom shape, which is preferably because of the desirable electrical characteristics a mushroom shaped gate provides. Providing a gate with a mushroom shape will help reduce intrinsic capacitance between the gate and the substrate 2, and will help reduce resistance between the gate and another electrode contacting the gate. However, those skilled in the art, will realize that the

presently disclosed technology may also be used to form structures wherein electrodes having a geometry other than a mushroom shape are deposited.

Optionally, after forming the gate foot region 4b, a recessed region 2b may be formed in the substrate 2, as shown in Fig. 2d-1. Those skilled in the art will realize that there are a variety of wet etches and dry etches which could be used to create the recessed region 2b in the substrate 2 using the existing resist layers 4, 6, 8 as a mask. Forming a gate in the recessed region 2b may help to improve the breakdown voltage characteristics of the device.

The gate contact region 6b and gate foot region 4b are then used as a mold wherein a metal gate will be formed using metal evaporation. Using the gate opening 8b as an entry point, metal for the gate is deposited in the gate contact region 6b and gate foot region 4b. Because the gate opening 8b defines the areas within the gate contact region 6b and gate foot region 4b which are covered with metal, it is important that the shape of the gate opening 8b does not change as a result of high temperatures. In depositing the metal, first an optional adhesion layer 16, shown in Fig. 3a-1, preferably approximately 20 Å thick, may be deposited in the gate foot region 4b on the surface 2a, and in the gate region 6b on the surface of the first resist layer 4 around the gate foot region 4b. The adhesion layer 16 preferably comprises titanium and helps promote adhesion of the gate to the surface 2a of the substrate. Also, in performing such a step, an extraneous adhesion layer (not shown) about 20 Å thick will also form on the exposed surface of the third resist layer 8, but will eventually be removed during the liftoff process (discussed later).

Next, a refractory metal layer 18 preferably about 400 Å thick is deposited on top of the adhesion layer (if deposited) in the gate foot region 4b and in the gate region 6b on the surface of the first resist layer 4 around the gate foot region 4b, as shown in Fig. 3a. The refractory metal layer 18 may comprise, for example, molybdenum or tungsten and can be deposited using a variety of known techniques, such as evaporation. An extraneous refractory metal layer 18a also forms on the surface of the extraneous

adhesion layer (if deposited). When the refractory metal layer 18 comprises molybdenum, for example, the temperature of the metal that forms in the mold is around 180°C. It is important that the gate foot region 4b maintain its shape during the deposition of the refractory metal layer 18. Electrical characteristics of the gate such as breakdown voltage and intrinsic capacitance are governed by the dimensions of the metal in the gate foot region 4b contacting the substrate 2. As a result, the gate foot region 4b must be able to maintain its shape in the first resist layer 4 during the metal evaporation of the adhesion layer 16 and refractory metal layer 18 in order to provide a gate foot with the desired dimensions.

Finally, a gate contact 20 having a thickness preferably about 4000 Å thick is deposited on the refractory metal layer 18 as shown in Fig. 3b. Gold is preferably used in the metal contact layer 18 because of its low resistance characteristics. The purpose of the refractory metal layer 18 is to prevent the gate contact 20 from diffusing into the substrate 2 during subsequent high temperature processing. For example, gold, which has a melting point around 1065° C, can still diffuse into the substrate 2 at room temperature. On the other hand, molybdenum, which has a melting point around 2620° C, will generally not diffuse into the substrate 2. In addition, it is also possible for the gate contact 20 to diffuse into the substrate 2 over time. The refractory metal layer 18 helps prevent this problem, thereby increasing the life span of the device. Those skilled in the art will realize that a gate having other dimensional parameters could be easily fabricated by using the aforementioned technique.

Once all the metal layers 16 (if used),18, and 20 have been applied, a lift-off process is performed to remove the remaining portions of the resist layers 4, 6, 8 by preferably using a solution of 1-methyl-2-pyrrolidinone (NMP) at 35 °C for 30–60 minutes, thereby leaving the gate contact 20 on the substrate 2, as shown in Fig. 3c.

Those skilled in the art should appreciate that the aforementioned techniques can be applied to fabricate other types of metal electrodes, such as an emitter contact

electrode for a heterojunction bipolar transistor or such as interdigitated electrodes for a metal-semiconductor photodetector, a photoconductive switch or a capacitor.

Various other alternative embodiments and/or modifications can be devised by those skilled in the art without departing from the spirit of this disclosure. Accordingly, the disclosed technology is intended to embrace all such alternatives, modifications, and variances that fall within the scope of the appended claims.